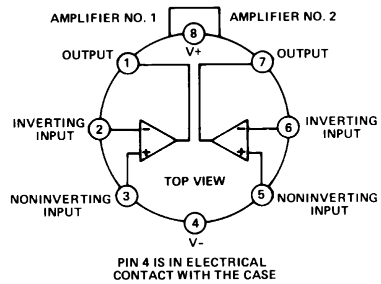
ANALOG DEVICES

Precision, Low Cost Dual BiFET Op Amp

AD642

FEATURES
Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Current
Crosstalk: –124 dB @ 1 kHz
Low Bias Current: 35 pA max Warmed Up
Low Offset Voltage: 500 μV max
Low Input Voltage Noise: 2 μV p-p
High Open Loop Gain
Low Quiescent Current: 2.8 mA max
Low Total Harmonic Distortion
Standard Dual Amplifier Pin Out
Available in Hermetic Metal Can Package and Chip Form
MIL-STD-883B Processing Available
Single Version Available: AD542

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD642 is a pair of matched high speed monolithic BiFET operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD642 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35 pA max matched to 25 pA for the AD642K and L; 75 pA max, matched to 35 pA for the AD642J and S. In addition, the offset voltage is laser trimmed to less than 0.5 mV and matched to 0.25 mV for the AD642L, 1.0 mV and matched to 0.5 mV for the AD642K, utilizing Analog's laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. The optimizes the process to product matched bias currents which have lower initial bias currents than other popular BiFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and combined with superior IC processing guarantees offset voltage tracking over the temperature range.

The AD642 is recommended for applications in which excellent ac and dc performance is required. The matched amplifiers provide a low-cost solution for true instrumentation amplifiers, log ratio amplifiers, and output amplifiers for four quadrant multiplying D/A converters such as the AD7541.

The AD642 is available in four versions: the "J", "K" and "L," all specified over the 0°C to +70°C temperature range and one version, "S," over the –55°C to +125°C extended operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can or available in chip form.

PRODUCT HIGHLIGHTS

1. The AD642 has tight matching specifications to ensure high performance, eliminating the need to match individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD642 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5 mV max and matched side to side to 0.25 mV (AD642L), thus eliminating the need for external nulling.
4. Low voltage noise (2 μV, p-p), and high open loop gain enhance the AD642's performance as a precision op amp.
5. The standard dual amplifier pin out allows the AD642 to replace lower performance duals without redesign.
6. The AD642 is available in chip form.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD642–SPECIFICATIONS (@ + 25°C, and V_S = ±15 V dc)

Model	AD642J Min	AD642J Typ	AD642J Max	AD642K Min	AD642K Typ	AD642K Max	AD642L Min	AD642L Typ	AD642L Max	AD642S Min	AD642S Typ	AD642S Max	Unit
OPEN LOOP GAIN													
V_O = ±10 V, R_L ≥ 2 kΩ	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{MIN} to T_{MAX}, R_L = 2 kΩ	100,000			**250,000**			**250,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 2 kΩ, T_{MIN} to T_{MAX}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ R_L = 10 kΩ, T_{MIN} to T_{MAX}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain	**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		V/µs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{MIN} to T_{MAX}			3.5			**2.0**			**1.0**			**3.5**	mV
Input Offset Voltage vs. Supply, T_{MIN} to T_{MAX}			**200**			**100**			**100**			**100**	µV/V
INPUT BIAS CURRENT[2]													
Either Input		10	75		10	35		10	35		10	35	pA
Offset Current		5			2			2			2		
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{MIN} to T_{MAX}			3.5			**2.0**			**1.0**			**3.5**	mV
Input Bias Current			**35**			**25**			**25**			**35**	pA
Crosstalk		–124			–124			–124			–124		dB
INPUT IMPEDANCE													
Differential		10^{12}‖6			10^{12}‖6			10^{12}‖6			10^{12}‖6		MΩ‖pF
Common Mode		10^{12}‖6			10^{12}‖6			10^{12}‖6			10^{12}‖6		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common-Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1 Hz to 10 Hz		2			2			2			2		µV p-p
f = 10 Hz		70			70			70			70		nV/√Hz
f = 100 Hz		45			45			45			45		nV/√Hz
f = 1 kHz		30			30			30			30		nV/√Hz
f = 10 kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±15	±5		±15	±5		±15	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TRANSISTOR COUNT		58			58			58			58		
PACKAGE OPTION													
TO-99 Style (H-08B)		AD642JH			AD642KH			AD642LH			AD642SH		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doublers every 10°C.

[3]Matching is defined as ther difference between parameters of the two amplifiers.

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10 V from ground.

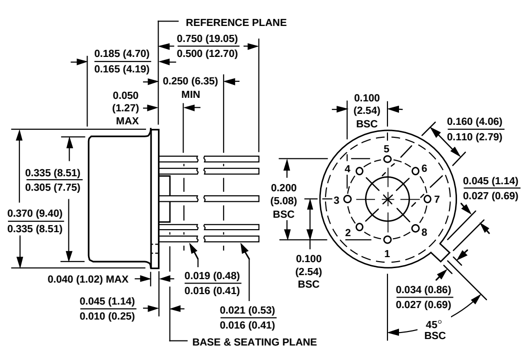
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

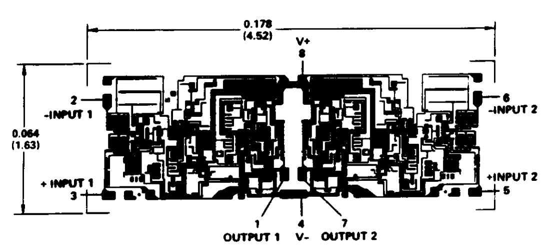
TO-99



METALIZATION PHOTOGRAPHIC

Contact factory for latest dimensions.

Dimensions shown in inches and (mm).



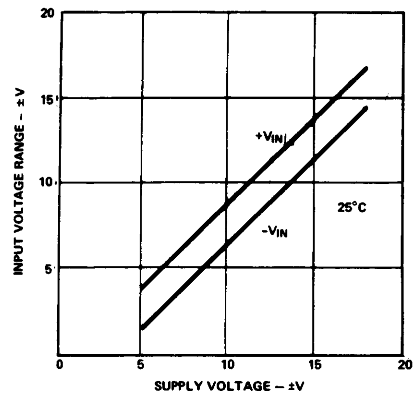


Figure 1. Input Voltage Range vs. Supply Voltage

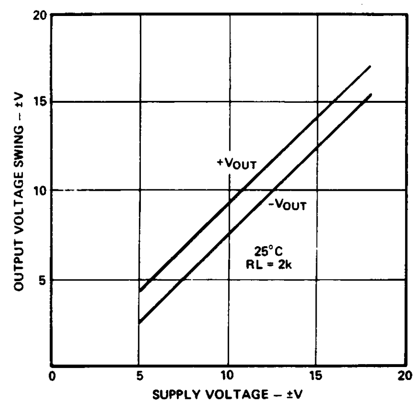


Figure 2. Output Voltage Swing vs. Supply Voltage

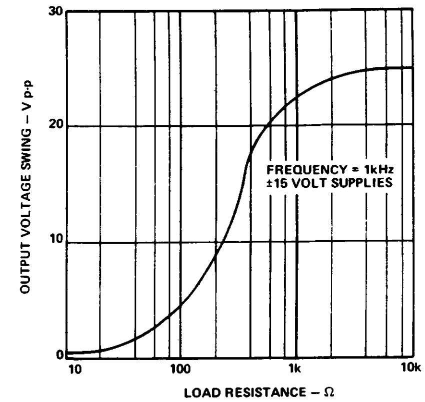


Figure 3. Output Voltage Swing vs. Load Resistance

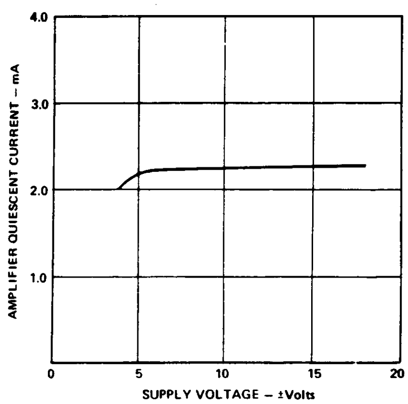


Figure 4. Quiescent Current vs. Supply Voltage

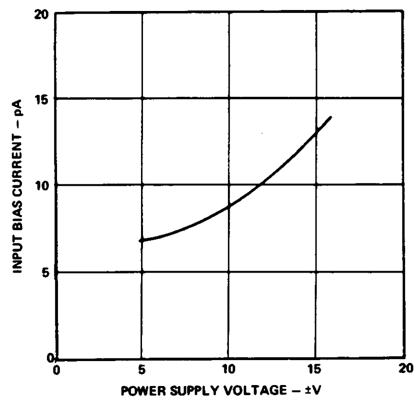


Figure 5. Input Bias Current vs. Power Supply Voltage

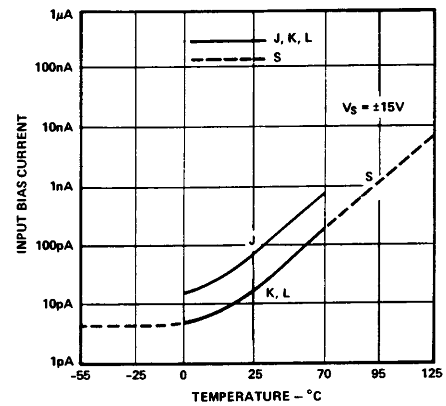


Figure 6. Input Bias Current vs. Temperature

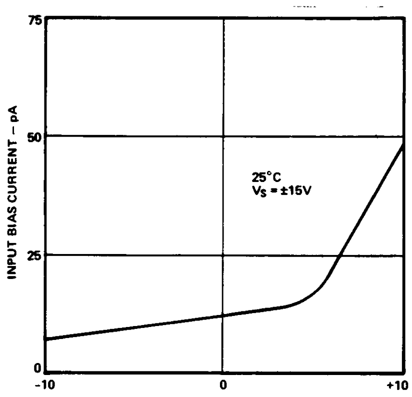


Figure 7. Input Bias Current vs. CMV

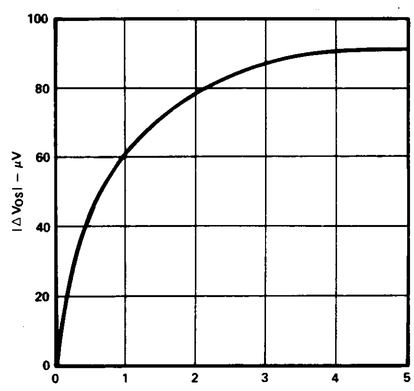


Figure 8. Change in Offset vs. Warm-Up Time

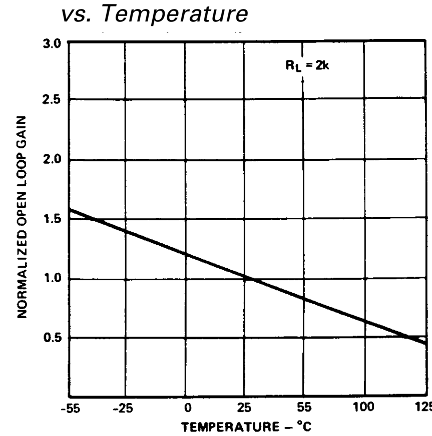


Figure 9. Open Loop vs. Temperature

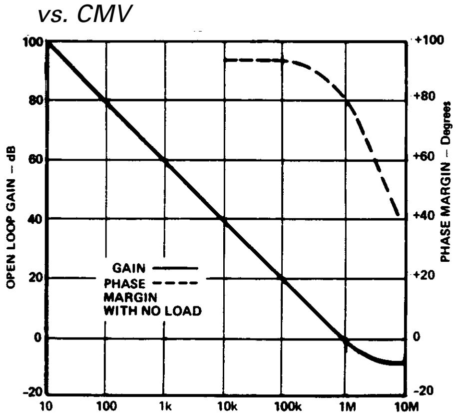


Figure 10. Open Loop Frequency Response

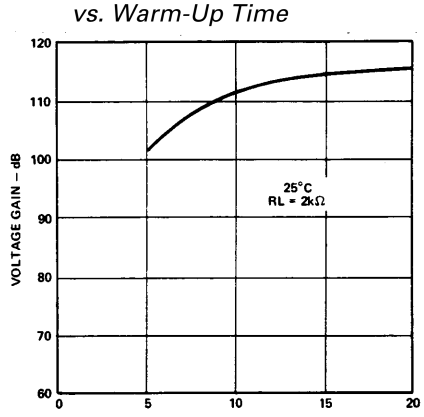


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

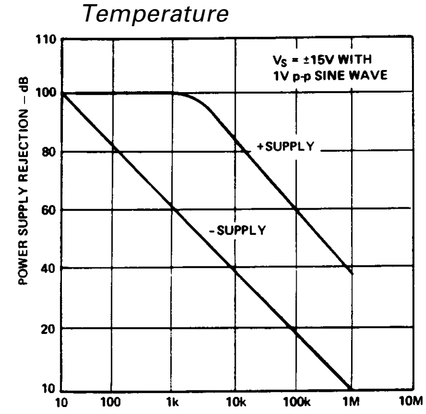


Figure 12. Power Supply Rejection vs. Frequency

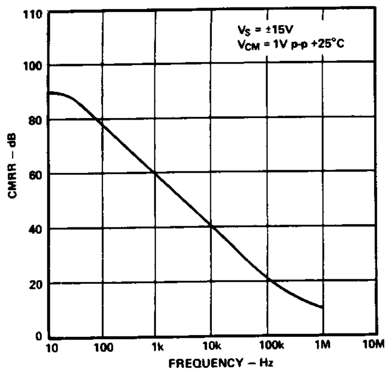


Figure 13. Common-Mode Rejection Ratio vs. Frequency

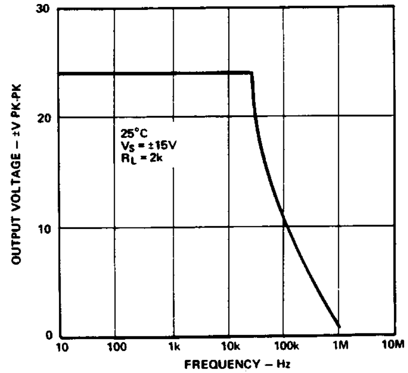


Figure 14. Large Signal Frequency Response

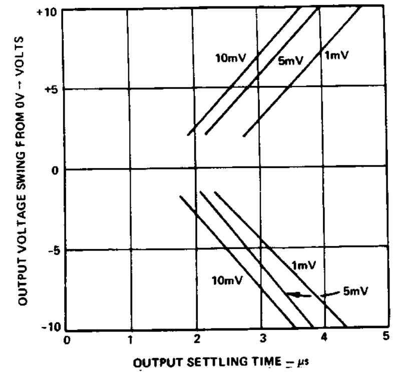


Figure 15. Output Swing and Error vs. Output Settling Time (Circuit of Figure 23)

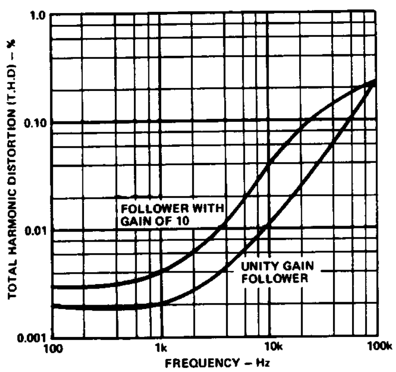


Figure 16. Total Harmonic Distortion vs. Frequency

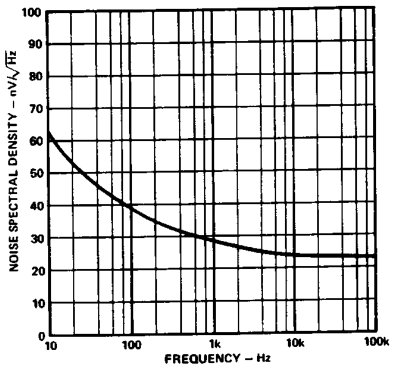


Figure 17. Input Noise Voltage Spectral Density

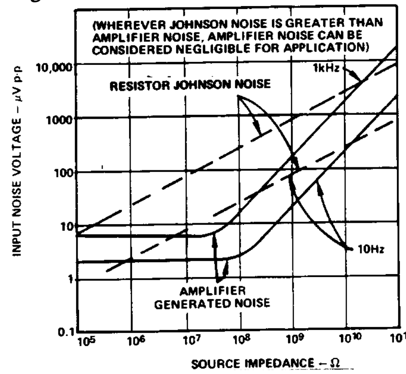
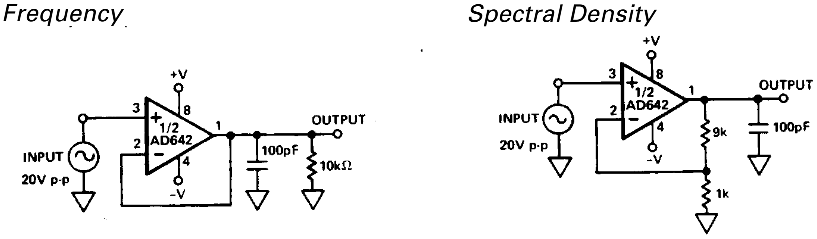


Figure 18. Total Noise vs. Source Impedance



a. Unity Gain Follower

b. Follower with Gain = 10

Figure 19. T. H. D. Test Circuits

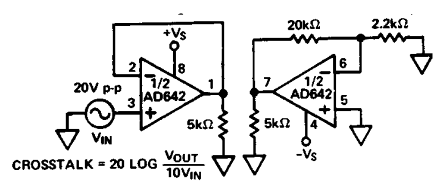


Figure 20. Crosstalk Test Circuit

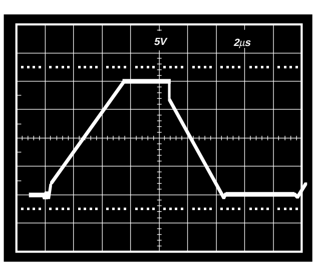


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

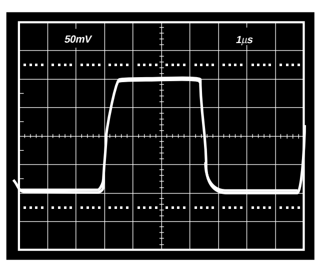


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

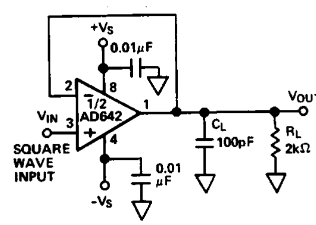


Figure 21c. Unity Gain Follower

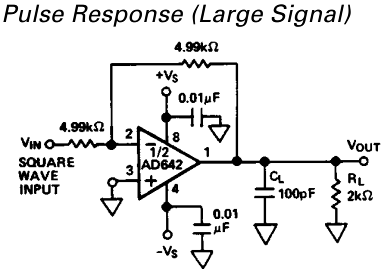


Figure 22a. Unity Gain Inverter

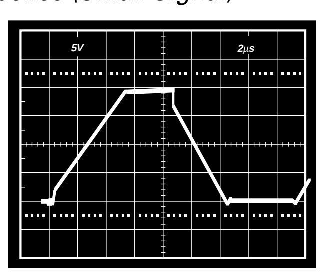


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

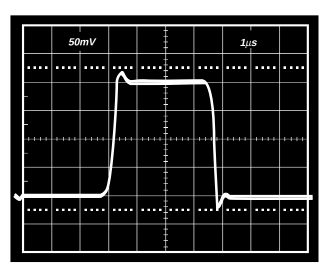


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

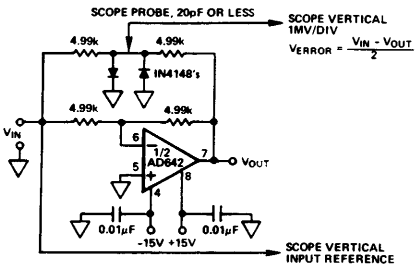


Figure 23. Settling Time Test Circuit

Fast settling time (8 µs to 0.01% for 20 V p-p step), low power and low offset voltage make the AD642 an excellent choice for use as an output amplifier for current output D/A converters such as the AD7541.

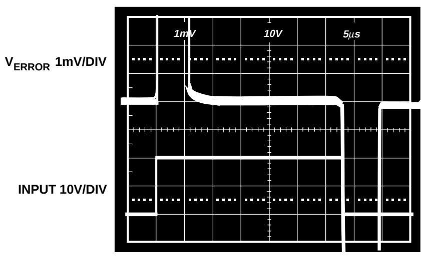
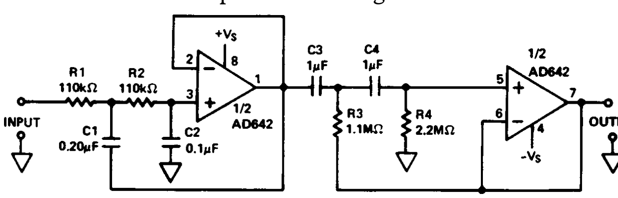


Figure 24. Settling Characteristic Detail

The upper trace of the oscilloscope photograph of Figure 24 shows the settling characteristic of the AD642. The lower trace represents the input to Figure 23. The AD642 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain optimum settling time.



R_1, R_2 = 1% METAL FILM RESISTOR NEED OR EQUIVALENT
C_1, C_2 = POLYPROP OR POLYCARB: 10% 50V
R_3, R_4 = 5% CARBON 1/4W, 1% METAL FILM PREFERRED
C_3, C_4 = LOW LKG, POLYPROPELENE, OR POLYCARB, 1µF, 5%, 50V MIN

Figure 25. 0.1 Hz to 10 Hz 2nd Order Bandpass Filter, Maximally Flat

The low frequency (1/f) noise has a power spectrum that is inversely proportional to frequency. Typically this noise is not important above 10 Hz, but it can be important for low frequency-high gain applications.

The low noise characteristic of the AD642 make it ideal for 1/f noise testing circuits. The circuit of Figure 25 is a 0.1 Hz to 10 Hz bandpass filter with second order filter characteristics.

The circuit illustrated in Figure 26 uses two AD642s to construct an instrumentation amplifier with low input current (35 pA max), high linearity and low offset voltage and offset voltage drift. The AD644 may be substituted for increased speed, but the higher open-loop gain of the AD642 maintains better linearity over the gain range of 1 to 1000. Amplifier A1 is an AD642L for low input offset voltage (250 µV max) and low input offset voltage drift at high gains because matching and tracking are very important for the balanced input stage. Amplifier A2 serves two nonrelated functions, output amplifier and active data-guard drive, and does not require close matching between sections; thus it may be an AD642J.

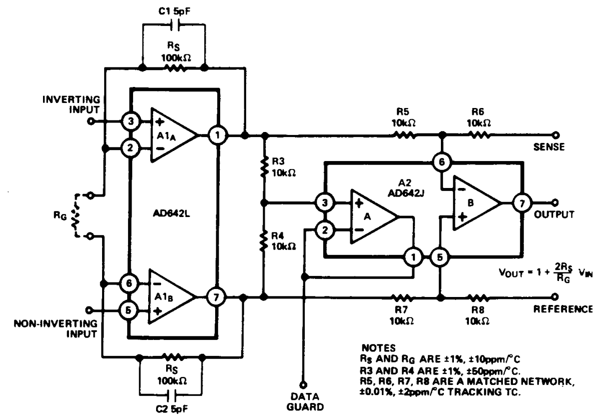
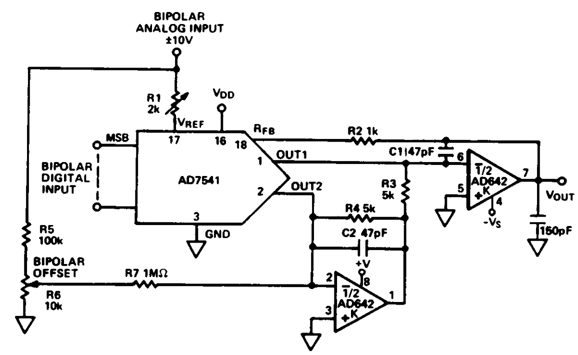


Figure 26. Precision FET Input Instrumentation Amplifier

The output impedance of a CMOS DAC varies with the digital word thus changing the noise of the amplifier circuit. This effect will cause a nonlinearity whose magnitude is dependent on the offset voltage of the amplifier. The AD642K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD642.



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED

Figure 27a. AD642 Used as DAC Output Amplifier

Figure 27a illustrates the AD7541 12-bit digital-to-analog converter, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplication.

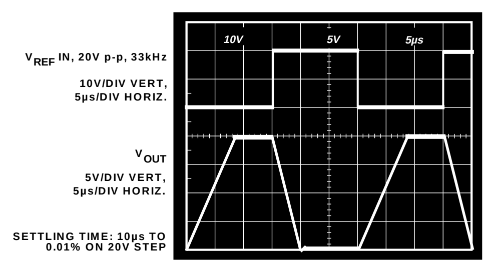


Figure 27b. Voltage Output DAC Settling Characteristic

The photo above shows the output of the circuit Figure 27a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC. The 47 pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150 pF load capacitor serves to minimize output glitches.

Log amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data,

linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multiterm products and ratios.

The picoamp level input current and low offset voltage of the AD642 make it suitable for wide dynamic range log amplifiers. Figure 28 is a schematic of a log ratio circuit employing the AD642 that can achieve less than 1% conformance error over 5 decades of current input, 1 nA to 100 µA. For voltage inputs, the dynamic range is typically 50 mV to 10 V for 1% error limited on the low end by the amplifier's input offset voltage.

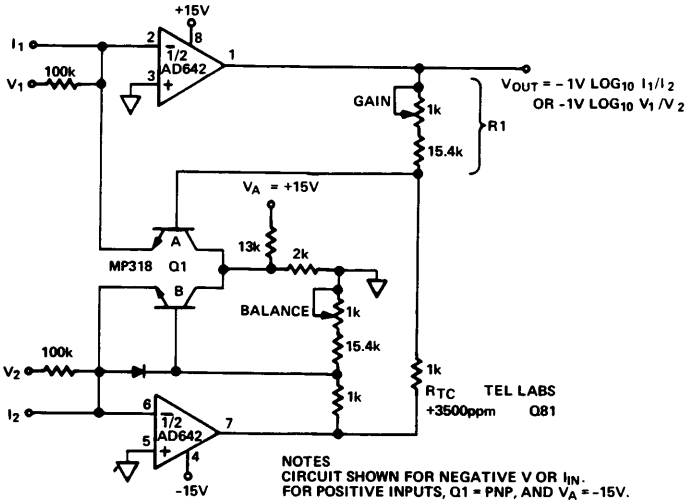


Figure 28. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has β>100, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the ratio of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\ kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1 V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500 ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The –3 dB bandwidth is 50 kHz over the top 3 decades, 100 nA to 100 µA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100 pF of shunt capacitance. For larger input capacitances a 20 pF integration capacitor around each amplifier will provide a smoother frequency response.

The log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = –10.00 V and adjust "Balance" for V_{OUT} = 0.00 V. Next apply V1 = –10.00 V, V2 = –1.00 V and adjust gain for V_{OUT} = +1.00 V. Repeat this procedure until gain and balance readings are within 2 mV of ideal values.

The low input bias current (35 pA) and low noise characteristics of the AD642 make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD642 can deliver. The input guarding scheme shown in Figure 29 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid shielded cables.

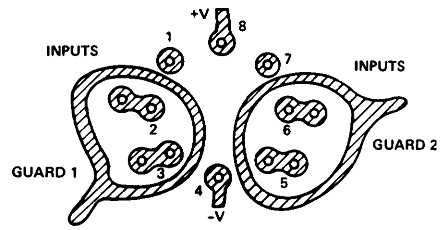


Figure 29. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD642 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±0.5 volts while maintaining the full differential input resistance of 10^{12} Ω. This makes the AD642 suitable for low speed voltage comparators directly connected to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate Zener protection schemes which often compromise overall performance. The AD642 requires input protection only if the source is not current limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0 mA (for example, 100 kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 30 shows proper connections.

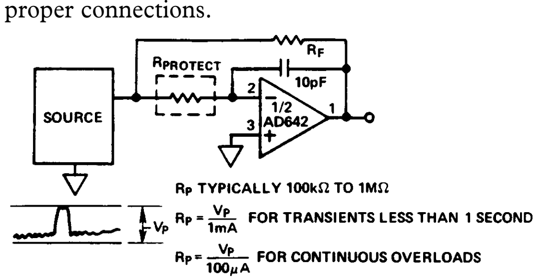


Figure 30. AD642 Input Protection

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